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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/717,737	11/20/2003	Huilong Zhu	YOR920030479US1	8704

33233 7590 06/30/2005

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EXAMINER	
SOWARD, IDA M	

ART UNIT	PAPER NUMBER
2822	

DATE MAILED: 06/30/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/717,737	ZHU ET AL.	
	Examiner	Art Unit	
	Ida M. Soward	2822	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *20 November 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-47* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-3,5-14,16 and 18-47* is/are rejected.

7)☒ Claim(s) *4,15 and 17* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *20 November 2003* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *11-20-2003*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

This Office Action is in response to the application filed November 20, 2003.

Drawings

The drawings are objected to because reference character "**202**" has been used to designate two different elements in Figure 3K. Corrected drawing sheets in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. Any amended replacement drawing sheet should include all of the figures appearing on the immediate prior version of the sheet, even if only one figure is being amended. The figure or figure number of an amended drawing should not be labeled as "amended." If a drawing figure is to be canceled, the appropriate figure must be removed from the replacement sheet, and where necessary, the remaining figures must be renumbered and appropriate changes made to the brief description of the several views of the drawings for consistency. Additional replacement sheets may be necessary to show the renumbering of the remaining figures. Each drawing sheet submitted after the filing date of an application must be labeled in the top margin as either "Replacement Sheet" or "New Sheet" pursuant to 37 CFR 1.121(d). If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 1-3, 6, 8-9, 14, 16, 19-20, 26 and 27-47 are rejected under 35 U.S.C. 103(a) as being unpatentable over Joshi et al. (US 2005/0017377 A1) in view of Fried et al. (US 2003/0178670 A1).

In regard to claim 1, Joshi et al. teach a field effect transistor (FET) comprising: a fin formed on a dielectric surface 22; a device gate 95 along one side of said fin; a back bias gate 96 along an opposite side of said fin; device gate dielectric 33 along one first side between said device gate 95 and said fin; and back bias gate dielectric 33 along said opposite side between said back bias gate 96 and said fin (Figure 8B, page 5, paragraphs [0045]-[0046]).

In regard to claim 14, Joshi et al. teach an integrated circuit (IC) on a semiconductor on insulator (SOI) chip 20, said IC including a plurality of field effect transistors (FETs) (one of many cells) disposed on an insulating layer 22, each of said FETS comprising: a semiconductor fin formed on an insulating layer 22; device gate dielectric 33 along a first side of said semiconductor fin; a device gate 95 along said device gate dielectric 33; back bias gate dielectric 33 along an opposite of said semiconductor fin; a back bias gate 96 along said back bias gate dielectric 33 (Figure 8B, page 5, paragraphs [0045]-[0046]).

In regard to claim 26, Joshi et al. teach a method of forming an integrated circuit (1C), said method comprising the steps of: a) forming semiconductor fins on a silicon on insulator (SOI) wafer 20; b) forming back bias gates 96 along one side of each of said semiconductor fins, said back bias gates 96 comprising back bias gate dielectric 33; and c) forming device gates 95 along an opposite side of each of said semiconductor fins (Figure 8B, page 5, paragraphs [0045]-[0046]).

However, Joshi et al. fail to teach a back bias gate dielectric differs from a device gate dielectric in at least one of material and thickness.

Fried et al. teach a back bias gate dielectric 116 differs from a device gate dielectric 110 in material (Figure 11, page 3, paragraphs [0031] and [0033]).

Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the field effect transistor structure as taught by Joshi et al. with the field effect transistor having a back bias gate dielectric differs from a device gate dielectric in material as taught by Fried et al. to provide capability for high density semiconductor devices (page 1, paragraph [0007]).

In regard to claims 2-3, Joshi et al. teach a silicon semiconductor fin (page 3, paragraph [0028]).

In regard to claims 6 and 16, Joshi et al. teach the back bias gate dielectric 33 and the gate dielectric 33 is selected from a group of materials consisting of an oxide and an oxynitride (page 3, paragraph [0031]).

In regard to claims 8 and 19, Joshi et al. teach the dielectric surface 22 is an oxide layer (page 3, paragraph [0028]).

In regard to claims 9 and 20, Joshi et al. teach the oxide layer 22 being a buried oxide layer (page 3, paragraph [0028]).

In regard to claims 27-47, claim 26 incorporates all the limitations of the device claims and the dependents claim also rejected as obvious in that the device structure as claimed could have been made by another and materially different process.

Claims 5, 7 and 18 are rejected under 35 U.S.C. 103(a) as being unpatentable over Joshi et al. (US 2005/0017377 A1) and Fried et al. (US 2003/0178670 A1) as applied to claims 1-3, 6, 8-9, 14, 16, 19-20, 26 and 27-47 above, and further in view of Yu (US 6,391,695 B1).

Joshi et al. and Fried et al. teach all mentioned in the rejection above.

However, Joshi et al. and Fried et al. fail to each a back bias gate dielectric being thicker than a gate dielectric.

In regard to claim 5, Yu teaches a back bias gate dielectric 22 being thicker than a gate dielectric 26 (Figure 10, columns 5-6, lines 13-67 and 1-33, respectively).

Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the field effect transistor structure as taught by Joshi et al. and the field effect transistor having a back bias gate dielectric differs from a device gate dielectric in material as taught by Fried et al. with the field effect transistor having a back bias gate dielectric being thicker than a gate dielectric as taught by Yu to manufacture smaller transistors to increase the component density on an integrated circuit (column 2, lines 7-9).

In regard to claims 7 and 18, Yu further teaches a gate 24 and a back bias gate 38 being a conductive material of doped silicon or doped germanium (Figure 10, columns 5-6, lines 36-51 and 25-33, respectively).

Claims 11, 22 and 25 are rejected under 35 U.S.C. 103(a) as being unpatentable over Joshi et al. (US 2005/0017377 A1) as applied to claims 1-3, 6, 8-9, 14, 16, 19-20, 26 and 27-47 above, and further in view of Fried et al. (US 2003/0178670 A1).

Joshi et al. teach all mentioned in the rejection above.

However, Joshi et al. fail to teach a dielectric pillar above a semiconductor silicon fin.

Fried et al. teach a dielectric pillar 102 above a semiconductor silicon fin 100 (Figure 11, page 3, paragraphs [0030] and [0038]).

Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the field effect transistor structure as taught by Joshi et al. with the field effect transistor having a dielectric pillar above a semiconductor silicon fin as taught by Fried et al. to allow horizontal current flow (abstract).

Claims 10, 12-13, 21 and 23-24 are rejected under 35 U.S.C. 103(a) as being unpatentable over Joshi et al. (US 2005/0017377 A1) and Fried et al. (US 2003/0178670 A1) as applied to claims 1-3, 6, 8-9, 14, 16, 19-20, 26 and 27-47 above, and further in view of Mathew et al. (US 2003/0151077 A1).

Joshi et al. and Fried et al. teach all mentioned in the rejection above.

However, Joshi et al. and Fried et al. fail to teach a dielectric pillar being a nitride pillar, and the nitride pillar forming a cap between a device gate and a back bias gate.

In regard to claims 12-13 and 23-24, Mathew et al. teach a dielectric pillar 22 being a nitride pillar, and the nitride pillar forming a cap between a gates 62' and 64' (Figure 15, pages 2-3, paragraphs [0017] and [0031], respectively).

Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the field effect transistor structure as taught by Joshi et al. and the field effect transistor having a back bias gate dielectric differs from a device gate dielectric in material as taught by Fried et al. with the field effect transistor having a dielectric pillar being a nitride pillar, and the nitride pillar forming a cap between a device gate and a back bias gate as taught by Mathew et al. to provide a device that is able to be made with reduced dimensions and still function at the required specifications (page 1, paragraph [0002]).

In regard to claims 10 and 21, Mathew et al. teach an oxide layer 14 disposed on a nitride layer 12 (Figure 15, page 1, paragraph [0016]).

Allowable Subject Matter

Claims 4, 15, 17 is objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Conclusion

The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

The following patent are cited to further show the state of the art with respect to FinFETs:

Dixit et al. (US 2005/0051812 A1)

Forbes (US 2004/0174734 A1)

Nowak et al. (US 6,888,199 B2)

Orlowski et al. (US 2005/0023616 A1)

Pham et al. (US 2004/0219722 A1)

Popp et al. (US 2005/0029583 A1)

Voldman (US 6,433,609 B1).

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Ida M. Soward whose telephone number is 571-272-1845. The examiner can normally be reached on Monday - Thursday 6:30am to 5:00pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Amir Zarabian can be reached on 571-272-1852. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

IMS
June 22, 2005

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